REMARKS

The Applicant sincerely appreciates the thorough examination of the present application as evidenced by the Office Actions of March 8, 2005, and August 18, 2005. In particular, the Applicant appreciates the Examiner's indication that Claims 1, 3-13, and 15-24 are allowed, and that Claims 42-49 would be allowable if rewritten in independent form.

In the following remarks, the Applicant will show that independent Claim 41 is patentable over the combination of Moyal and Rhyne. Accordingly, dependent Claims 42-49 (all indicated allowable) have not been rewritten in independent form. All pending claims are, thus, patentable over the cited art, and a Notice of Allowance is respectfully requested in due course.

Consideration Of Art Cited With Information Disclosure Statement Is Requested

The Applicant respectfully requests that the Examiner provide indication of consideration of the references cited with the Applicant's Information Disclosure Statement that was filed on June 7, 2005. Copies of the Information Disclosure Statement (including a Certificate Of Mailing dated June 7, 2005), the Form PTO-1449 (citing 7 references), and the post card receipt (showing receipt at the U.S. Patent Office on June 9, 2005) are attached hereto for the Examiner's convenience. Accordingly, the Applicant respectfully requests that the Examiner return a copy of the Form PTO-1449 (with each reference citation initialed) to reflect consideration of the cited references. At the Examiner's request, copies of the cited references will be retransmitted.

Claim 41 Is Patentable Over Moyal

Claim 41 has been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,329,840 to Moyal ("Moyal") in view of the reference by Rhyne (Fundamentals Of Digital System Design, N.J., 1973, pp. 70-71). Claim 41, however, is patentable over the combination of Moyal and Rhyne for at least the reasons discussed below. In particular, Claim 41 recites an output buffer circuit including:

> a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives at least one control signal and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the control signal and the data and generates the pull-down control signal,

wherein a number of PMOS transistors present along a path of a first supply voltage to an output terminal of the NAND gate is equivalent to a number of PMOS transistors present along a path of the first supply voltage to an output terminal of the NOR gate, and a number of NMOS transistors present along a path of a second supply voltage to an output terminal of the NAND gate is equivalent to a number of NMOS transistors present along a path of the second supply voltage to an output terminal of the NOR gate.

The Final Office Action concedes that Moyal fails to teach or suggest a NAND gate generating a pull-up control signal or a NOR gate generating a pull-down control signal. The Applicant submits that Rhyne fails to provide the missing teachings. In particular, the Final Office Action states that:

> ... Moyal discloses the claimed invention except for the NAND gate connected to the pull-up transistor and the NOR gate connected to the pull-down transistor instead of the NOR gate connected to the pull-up transistor and the NAND gate connected to the pull-down transistor.
>
> Rhyne teaches a function of any one of the four logical functions, AND, OR, NAND, or NOR, can be redefined so as to perform the other three (Fig. 3-10), these function is equivalent structure known in the art.
>
> Therefore, because these two gate function as NOR gate or NAND gate were art-recognized equivalents at the time the invention was made, one or ordinary skill in the art would have found it obvious to substitute the NAND gate connected to the pull-up transistor and the NOR gate connected to the pull-down transistor for the NOR gate connected to the pull-up transistor and the NAND gate connected to the pull-down transistor.

Office Action, pages 2-3.

The Applicant respectfully submits that NOR and NAND gates are not equivalent as set forth in the Applicant's Amendment of June 7, 2005. More particularly, NOR and NAND gates

provide functionality according to the truth tables set forth below:

NOR Gate			NAND Gate		
Inputs		Output	Inputs		Output
A	B	X	A	B	Y
0	0	1	0	0	1
0	1	0	0	1	1
1	0	0	1	0	1
1	1	0	1	1	0

Accordingly, the functionalities of NOR and NAND gates are not equivalent. As stated in Rhyne, NAND/NOR functions form a reversed symbolism pair. More particularly, the functionality of a NOR gate may be provided by adding inverters to all inputs and the output of a NAND gate, and the functionality of a NAND gate may be provided by adding inverters to all inputs and the output of a NOR gate. Stated again, the functionalities of NOR and NAND gates are not equivalent.

Accordingly, it would not be obvious to somehow switch the NOR and NAND logic gates of Moyal, and if such a switch were made, there is no reasonable expectation that the resulting circuit would perform the function intended by Moyal. As set forth in the Manual Of Patent Examining Procedure (MPEP), three basic criteria must be met to establish a *prima facie* case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Moreover, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP, Sec. 2143.

More particularly, switching the NOR and NAND gates of Moyal would result in a circuit that does not perform its intended function because NOR and NAND gates perform different functionalities. In fact, Moyal teaches away from substitution of a NAND gate with input and output inventers to perform a NOR function, and substitution of a NOR gate with input and output inverters to perform a NAND function, because such substitutions would change the

timing of the circuits of Moyal, and Moyal states as its object to provide control signals matched to control the timing of the output transistors. More particularly, Moyal states that:

> The objects, features and advantages of the present invention include providing a circuit, architecture, and method for implementing a tri-state output buffer with control signals matched to control the timing of the output transistors.

Moyal, col. 2, lines 1-4. Moyal thus teaches away from changing the circuits **128a** and/or **128b** of Figure 7 of Moyal as suggested by the Final Office Action, because the object of circuits of Moyal is to provide "control signals matched to control the timing of the output transistors," and changes suggested in the Final Office Action would provide different timing.

For at least the reasons discussed above, the Applicant respectfully submits that the combination of Moyal and Rhyne fails to teach or suggest the output buffer circuit of Claim 41, and that Claim 41 is thus patentable. The Applicant further submits that dependent Claims 42-49 are patentable at least as per the patentability of Claim 41 from which they depend. Dependent Claims 42-49 are also independently patentable as set forth on page 3 of the Office Action.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

Respectfully submitted,

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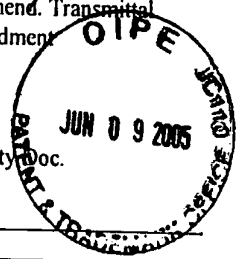

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